What is claimed is:

1. A method for reducing Critical Dimension (CD) non-uniformity in creating a patterned layer of semiconductor material, comprising:

providing a substrate, said substrate having been provided with one or more layers of semiconductor material;

depositing a first masking layer over one or more layers of semiconductor material;

creating, while applying methods for compensation of optical proximity effects and micro-loading, a first pattern in said first masking layer, said first pattern being a pattern of high-density semiconductor device features and isolated semiconductor device features and dummy features;

patterning at least one of said one or more layers of semiconductor material in accordance with said first pattern;

removing said first masking layer;

depositing a second masking layer over said at least one layer of semiconductor material, including said patterned at least one of said one or more layers of semiconductor material;

creating a second pattern in said second masking layer, said second pattern exposing dummy features of said patterned at least one of said one or more layers of semiconductor material;

patterning said at least one layer of semiconductor material in accordance with said second pattern; and

removing said second masking layer.

2. The method of claim 1, said creating while applying methods for compensation of optical proximity effects and micro-loading a first pattern in said first masking layer comprising:

first exposing said first masking layer with a first mask, said first mask comprising a first and a second pattern, said first pattern being a pattern of high-density semiconductor device features having a first cross-section, said second pattern being full-size assist features having a second cross-section, said full-size assist features being designed to maximize contribution to spatial frequency and to achieve unification of an exposure level of the high-density device features;

second exposing said first masking layer with a second mask, said second mask comprising a third pattern, said third pattern aligning with said second pattern on said first mask; and

etching said first masking layer in accordance with said first and second exposure of said masking layer.

3. The method of claim 2, said third pattern having dimensions being larger than dimensions of said second pattern by a measurable amount.

4. The method of claim 2, a distance between elements of said full-size assist feature and elements of said high-density semiconductor device features being within a range of between about 0.5 and 3.0 times said cross-section of said high-density semiconductor device features.

5. The method of claim 2, said first cross-section being about equal to said second cross-section.

6. The method of claim 2, a distance between elements of said full-size assist feature and elements of said high-density semiconductor device features and said isolated features and said dummy features being determined by first independent parameters, said first independent parameters being dimensions of said high-density semiconductor device features, said first independent parameters having as objective maximization of said contribution to spatial frequency and to achieving unification of an exposure level of the high-density device features by said full-size assist features, thereby assuring optimum imaging performance.

7. The method of claim 2, a design of said full-size assist feature being determined by second independent parameters, said second independent parameters being dimensions of said high-density semiconductor device features, said second independent

parameters having as objective maximization of said contribution to spatial frequency and to achieving unification of an exposure level of the high-density device features by said full-size assist features, thereby assuring optimum imaging performance.

8. The method of claim 2, said first masking layer comprising photoresist.

9. The method of claim 2, said first and said second pattern comprising an opaque surface region of said first mask surrounded by a transparent background surface region.

10. The method of claim 2, said first and said second pattern comprising a transparent surface region of said first mask surrounded by an opaque background surface region.

11. The method of claim 2, said third pattern comprising an opaque surface region of said first pattern surrounded by a transparent background surface region.

12. The method of claim 2, said third pattern comprising a transparent surface region of said first pattern surrounded by an opaque background surface region.

13. The method of claim 2, said first masking layer comprising an insulating material.

14. The method of claim 2 wherein overlapping full-size assist features of said second pattern of full-size assist features are combined into larger full-size assist features.

15. The method of claim 2 wherein said second pattern comprises side-by-side full-size assist features.

16. The method of claim 2, said third pattern being aligned with said first pattern, keying said third pattern to said first pattern.

17. The method of claim 2, elements of said second pattern being interspersed with elements of said first pattern.

18. The method of claim 2, elements of said second pattern surrounding elements of said first pattern.

19. The method of claim 1, said second masking layer comprising photoresist.

20. The method of claim 1, said at least one layer of semiconductor material being a layer of dielectric, a layer of insulating material, a layer of passivation material, a layer of hardmask material or a layer of conductive material.

21. The method of claim 1, said high-density semiconductor device features being separated by a distance of 2.0 μm or less.

22. The method of claim 1, said isolated semiconductor device features being separated from adjacent pattern features by a distance of 2.0 μm or less.

23. The method of claim 1, said dummy features being separated from adjacent high-density semiconductor device features or isolated semiconductor device by a distance of 2.0 μm or less.

24. A system for reducing Critical Dimension (CD) non-uniformity in creating a patterned layer of semiconductor material, comprising:

a Central Processing Unit (CPU) to which are connected, via data links, means of data entry and data extraction and data storage devices, the CPU further being connected to semiconductor processing tools and more specifically being connected to

photolithographic exposure tools applied for creation of semiconductor devices;

a software support function for creating, while applying methods for compensation of optical proximity effects and micro-loading, a first pattern in a first masking layer over one or more layers of semiconductor material having been provided over a substrate, said first pattern being a pattern of high-density semiconductor device features and isolated semiconductor device features and dummy features, said first masking layer being applied for patterning at least one of said one or more layers of semiconductor material in accordance with said first pattern after which said first masking layer is removed;

a software support function for creating a second pattern in a second masking layer provided over said at least one layer of semiconductor material, including said patterned at least one of said one or more layers of semiconductor material, said second pattern exposing dummy features of said patterned at least one of said one or more layers of semiconductor material, said second pattern being applied for patterning said at least one layer of semiconductor material after which said second masking layer is removed.

25. The system of claim 24, said creating while applying methods for compensation of optical proximity effects and micro-loading a first pattern in said first masking layer comprising:

means for first exposing said first masking layer with a first mask, said first mask comprising a first and a second pattern, said first pattern being a pattern of high-density semiconductor device features having a first cross-section, said second pattern being full-size assist features having a second cross-section, said full-size assist features being designed to maximize contribution to spatial frequency and to achieve unification of an exposure level of the high-density device features;

means for second exposing said first masking layer with a second mask, said second mask comprising a third pattern, said third pattern aligning with said second pattern on said first mask; and

means for etching said first masking layer in accordance with said first and second exposure of said masking layer.

26. The system of claim 25, said third pattern having dimensions being larger than dimensions of said second pattern by a measurable amount.

27. The system of claim 25, a distance between elements of said full-size assist feature and elements of said high-density semiconductor device features being within a range of between about 0.5 and 3.0 times said cross-section of said high-density semiconductor device features.

28. The system of claim 25, said first cross-section being about equal to said second cross-section.

29. The system of claim 25, a distance between elements of said full-size assist feature and elements of said high-density semiconductor device features and said isolated features and said dummy features being determined by first independent parameters, said first independent parameters being dimensions of said high-density semiconductor device features, said first independent parameters having as objective maximization of said contribution to spatial frequency and to achieving unification of an exposure level of the high-density device features by said full-size assist features, thereby assuring optimum imaging performance.

30. The system of claim 25, a design of said full-size assist feature being determined by second independent parameters, said second independent parameters being dimensions of said high-density semiconductor device features, said second independent

parameters having as objective maximization of said contribution to spatial frequency and to achieving unification of an exposure level of the high-density device features by said full-size assist features, thereby assuring optimum imaging performance.

31. The system of claim 25, said first masking layer comprising photoresist.

32. The system of claim 25, said first and said second pattern comprising an opaque surface region of said first mask surrounded by a transparent background surface region.

33. The system of claim 25, said first and said second pattern comprising a transparent surface region of said first mask surrounded by an opaque background surface region.

34. The system of claim 25, said third pattern comprising an opaque surface region of said first pattern surrounded by a transparent background surface region.

35. The system of claim 25, said third pattern comprising a transparent surface region of said first pattern surrounded by an opaque background surface region.

36. The system of claim 25, said first masking layer comprising an insulating material.

37. The system of claim 25 wherein overlapping full-size assist features of said second pattern of full-size assist features are combined into larger full-size assist features.

38. The system of claim 25 wherein said second pattern comprises side-by-side full-size assist features.

39. The system of claim 25, said third pattern being aligned with said first pattern, keying said third pattern to said first pattern.

40. The system of claim 25, elements of said second pattern being interspersed with elements of said first pattern.

41. The system of claim 25, elements of said second pattern surrounding elements of said first pattern.

42. The system of claim 24, said second masking layer comprising photoresist.

43. The system of claim 24, said at least one layer of semiconductor material being a layer of dielectric, a layer of

insulating material, a layer of passivation material, a layer of hardmask material or a layer of conductive material.

44. The system of claim 24, said high-density semiconductor device features being separated by a distance of 2.0 μm or less.

45. The system of claim 24, said isolated semiconductor device features being separated from adjacent pattern features by a distance of 2.0 μm or less.

46. The system of claim 24, said dummy features being separated from adjacent high-density semiconductor device features or isolated semiconductor device by a distance of 2.0 μm or less.